Closed-loop Control of High Frequency AC PWM Inverter for Space Application

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***Abstract*—This paper presents a closed-loop controller design approach for a single-phase (1ϕ) pulse-width modulated (PWM) high frequency (HF) AC inverter, supplying the non-linear load for space application. Control challenges in HF inverter are highlighted compared with 50/60 Hz conventional inverter. Considering HF PWM inverter with resistive load, the parameters for two-loop control structure are decided to meet specific stability criteria and steady-state performance. Re-tuning of the controller is performed to support non-linear load (uncontrolled diode bridge rectifier) with trap filters. The possibility of connecting damper resistors in series with the trap filters is also explored for better control loop shaping. Analog realization of the controller is also discussed in brief. The proposed controller design is validated experimentally by transferring 0.5 kW power through a 50 V peak, 10 kHz AC system.**

***Index Terms*—High frequency AC system, space application, nested loop control, resonant controller.**

I. Introduction

The conventional DC distribution system for satellites comprises multiple DC-DC stages followed by point-of-load (POL) converters, as shown in Fig. 1a. A large number of isolated DC-DC converters increase productization costs and challenges. A potential solution to these problems can be a high-frequency AC (HFAC) distribution system, as shown in Fig. 1b. In this system, the HF inverter forms an AC bus. At the load end, high-frequency transformers (HFTs), followed by simple diode bridge rectifiers, are used to feed the POLs. This configuration overcomes the limitations of the DC distribution system [1], [2].

The resonant mode power conversion approach was adopted in classical HF inverters so that the switching frequency can equal the power-line frequency. The lack of fast switching devices primarily drove this type of approach. Both Thyristor-based Mapham's inverter [3] and MOSFET-based series-parallel [4] topology rely on the parallel resonance of the tank network. But due to the load-dependent voltage gain property of parallel resonant tank, output voltage control in these inverters demands a large variation in switching frequency. Though this is avoided using a pre-regulator buck stage [4] before the resonant inverter, the simplicity of the original topology is compromised.

Due to its inherent load-independent voltage gain property, pulse-width-modulated (PWM) inverter can be a suitable alternative for this application. Though a PWM inverter needs to be switched at a frequency at least 20 times higher than the power-line frequency, this is achievable using current power semiconductor devices. In this approach, the PWM inverter forms a 50 V_{pk}, 10 kHz AC bus, as shown in Fig. 1b, and the diode rectifier draws square-wave current from it. Trap filters are used to supply the higher-order current harmonics to the load. Thus good quality current and voltage waveforms at HFAC bus are maintained. Moreover, well-established output voltage control techniques for 50/60 Hz inverters could potentially be extended to HFAC PWM inverters.

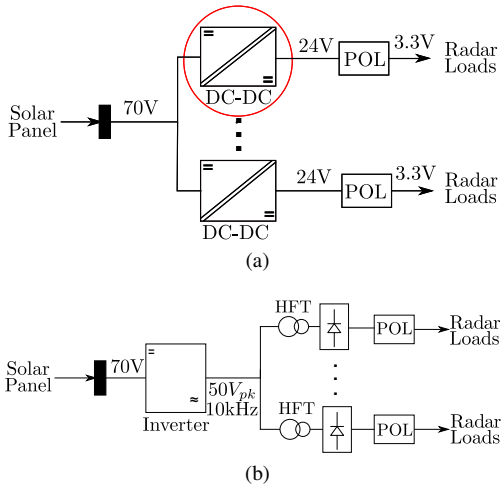


Fig. 1. (a) DC and (b) HFAC power system.

The nested 2-loop control structure is typically adopted for standalone 50/60 Hz single phase (1ϕ) PWM inverters. A fast inner loop controls the filter inductor current, and a slow outer loop regulates the filter capacitor voltage [5]. Different controller options [6] applicable to both current and voltage loops are summarized in Table I. Due to finite gain at 50/60 Hz, the PI controller does not ensure zero steady-state error for AC systems. To use this controller, the stationary frame variables need to be transformed into the synchronous (DQ) reference frame [7]. But this transformation requires an additional signal in quadrature with the reference, which increases circuit overhead for analog realization [8]. PR1 controller [9], given in Table I is directly used in the stationary frame, which provides infinite gain at the fundamental frequency that

TABLE I
DIFFERENT CONTROLLER TRANSFER FUNCTIONS.

PI	$\frac{K_i\left(\frac{s}{K_i/K_P}+1\right)}{s}$
Proportional-Resonant (Type-1), PR1	$K_p + \frac{K_i/\omega_o^2}{(s/\omega_o)^2+1}$
Proportional-Resonant (Type-2), PR2	$K_p + \frac{K_i s/\omega_o Q_H}{(s/\omega_o)^2+(s/\omega_o Q_H)+1}$

ensures zero steady-state error. Since the controller transfer characteristic is extremely narrow around the fundamental frequency, a slight deviation in control circuit components significantly affects the closed-loop performance. On the other hand, PR2 controller [10] gives the flexibility to tune the width of the notch around the fundamental frequency (ω_o) in terms of quality factor (Q_H), and thus makes the control loop immune to component tolerances. This controller offers finite gain at the fundamental frequency, which can be decided based on desired steady-state error.

It should be noted that, in 50/60 Hz, 1ϕ PWM inverters are typically switched at 10 kHz with LC filter corner frequency at 1 kHz. This gives a sufficient window to position the gain crossover frequency of the fast inner current loop. But HF PWM inverter cannot be switched at a very high frequency due to practical constraints on power loss. This narrows down the gap between fundamental (10 kHz) and LC corner frequency (30 kHz), making the controller design quite challenging. Moreover, trap filters with non-linear load make the plant transfer function higher to complicate the control loop further.

This paper presents a structured closed-loop controller design approach for HFAC 1ϕ PWM inverter. The key contributions of this paper are as follows. (a) Systematic design of 2-loop control architecture for 1ϕ HF inverter with resistive load is detailed. (b) The required modifications in the control loop due to the presence of trap filters and non-linear load are discussed. (c) The possibility of connecting damper resistances in series with the trap filters for better control loop shaping is explained. (d) Analog realization of the resonant controller is also presented.

The organization of the paper is as follows: Section II presents the power circuit and the controller architecture; Sections III and IV discuss the closed-loop control with resistive and non-linear load, respectively; the analog implementation of the resonant controller and the validation of the proposed control structure are discussed in Sections V and VI, respectively; finally, the paper is concluded in Section VII.

II. POWER CIRCUIT AND CONTROL ARCHITECTURE

The complete power architecture of single phase (1ϕ) HFAC PWM inverter is presented in Fig. 2, where V_{DC} is the input DC bus voltage. L_f and C_f are the inverter side filter inductor and capacitor, respectively. The lumped value of total line inductance is presented as L_l. The rectifier side filter inductor and capacitor are denoted by L_{fDC} and C_{fDC}, respectively. As the diode bridge rectifier draws square-wave current, i_{DB}, odd-harmonic trap filters up to order ninth are used so that near sinusoidal current is drawn from the single-phase inverter. Since any leakage inductance gets absorbed in L_l, the high-frequency transformer (HFT) is not considered here without

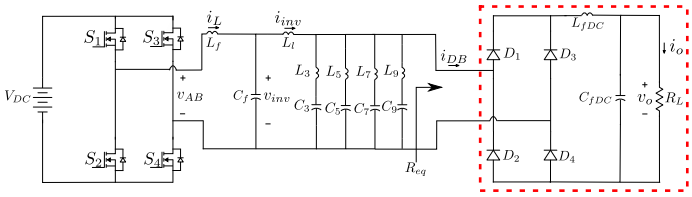


Fig. 2. Complete power train of a PWM inverter module.

TABLE II
SPECIFICATION OF PWM INVERTER

Parameters	Value	Parameters	Value	Parameters	Value	Parameters	Value
V_{DC}	70 V	L_f	10.4 μH	L_5	15.788 μH	C_9	0.628 μF
$v_{inv(peak)}$	50 V	C_f	1.25 μF	C_5	0.611 μF	L_{fDC}	54 μH
f_o	10 kHz	L_l	3.3 μH	L_7	8.96 μH	C_{fDC}	40 μF
f_s	200 kHz	L_3	50.92 μH	C_7	0.6237 μF	R_L	1.95 Ω
P_o	500 W	C_3	0.566 μF	L_9	4.96 μH	R_eq	2.41 Ω

any loss of generality. The concentrated load, R_L, is reflected across the trap filters as $R_{eq} = \frac{\pi^2}{8} R_L$ [12]. The specification of the power circuit is given in Table II, where f_o and f_s are the fundamental and switching frequencies, respectively. P_0 denotes rated output power.

Nested loop control structure for HFAC inverter is shown in Fig. 3. Here, an outer loop for output voltage (v_{inv}) control is followed by an inner inductor current (i_L) control loop. $H_i(s)$ and $H_v(s)$ are the current and voltage sensor transfer functions, respectively. Resonant type controllers, derived from the conventional PR2 transfer function, as given in Table I, are used for both current and voltage loops. The design specification for both the loops are as follows,

- To ensure the stability, phase margins for both the loops should be at least 50^o.
- Steady-state error needs to be minimized without compromising the stability.
- Typically the quality factor of resonant controller is restricted up to 10 due to limitations in analog implementation of the controller [11].

III. CLOSED-LOOP CONTROLLER DESIGN WITH RESISTIVE LOAD

A preliminary controller design is performed considering only the reflected load resistance (R_{eq}) across the diode bridge. For this simplified design, the trap filters are ignored.

A. Design of Current Controller

The control block diagram for the current loop is shown in Fig. 4, where $G_i(s)$ represents the plant transfer function, expressed as (1). Here, C_f is in parallel with the series

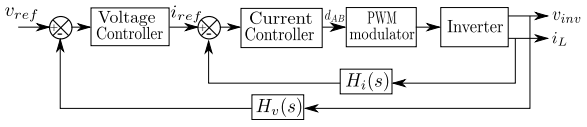


Fig. 3. Nested control loop for HF PWM inverter.

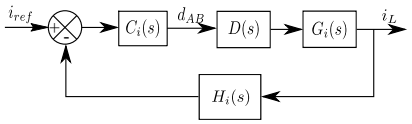
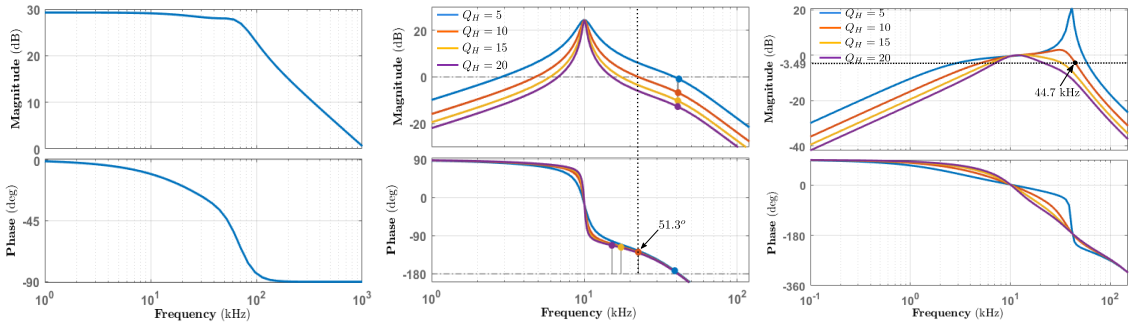


Fig. 4. Control block diagram for the inner current loop.



(a) $G_i(s)$ (b) $C_i(s)G_i(s)D_i(s)H_i(s)$ (c) $G_{CL}(s)$

Fig. 5. Frequency response of various control transfer functions for the current loop.

combination of R_{eq} and L_l. This impedance is in series with the L_f. Frequency response of $G_i(s)$ is presented in Fig. 5a. The PWM modulator with analog implementation is represented by a delay, $D(s) = e^{(-sT_s/2)}$, where T_s is the switching time period of 5 μs. The current sensor ($H_i(s)$) is modeled as a low pass filter with the corner frequency, ω_p =250 kHz and gain, $\alpha_i = 0.184$, expressed in (2).

C_i represents the current controller, given by (3), where K_i and Q_H are the gain and quality factor, respectively. The resonant frequency of the controller is tuned at HFAC line frequency (ω_o= $2\pi 10$ krad/s). The closed-loop transfer function of the current loop is expressed as (4).

$$G_i(s) = \frac{i_L(s)}{d_{AB}(s)} = \frac{V_{DC}}{L_f} \frac{s^2 + \frac{R_{eq}}{L_l}s + \frac{1}{L_l C_f}}{s^3 + \frac{R_{eq}}{L_f}s^2 + \frac{1}{L_{eq}C_f}s + \frac{R_{eq}}{L_f L_l C_f}}, \; L_{eq} = L_f || L_l \quad (1)$$

$$H_i(s) = \frac{\alpha_i}{1 + s/\omega_p} \quad (2) \qquad C_i(s) = \frac{K_i \frac{s}{\omega_o Q_H}}{(\frac{s}{\omega_o})^2 + \frac{s}{\omega_o Q_H} + 1} \quad (3)$$

$$G_{CL}(s) = \frac{i_L(s)}{i_{ref}(s)} = \frac{G_i(s)C_i(s)D(s)}{1 + C_i(s)G_i(s)D(s)H_i(s)} \quad (4)$$

Considering a scaling factor in the current reference, which is equal to the sensor gain (α_i), an expression for the steady-state error (SS) is derived as (5). Since the controller offers only a gain, K_i at ω_0 i.e., $|C_i|_{s=j\omega_o} = K_i$, (5) is rearranged as (6). Here, $|G_i|$ is the gain of the current plant at ω_o. Similarly, $\angle G_i$, $\angle H_i$ and $\angle D$ are the phase contributions of the current plant, current sensor and modulator at fundamental frequency, respectively. Using (6), for 5% steady-state error at ω_o=10 kHz, K_i for current controller is decided as 3.

$$1 - SS = \left| \frac{i_L \alpha_i}{i_{ref}} \right|_{(s=j\omega_o)} = \left| G_{CL}(s)\alpha_i \right|_{(s=j\omega_o)} \quad (5)$$

$$K_i = \frac{-cos(\angle G_i + \angle D + \angle H_i) \pm \sqrt{cos^2(\angle G_i + \angle D + \angle H_i) + (\frac{1}{SS})^2 - 1}}{|G_i|\alpha_i} \quad (6)$$

For a known value of K_i, Q_H is decided from the phase margin (PM) and bandwidth (BW) considerations. Fig. 5b and Fig. 5c show the bode plots of loop gain and closed loop transfer functions of the current loop at different values of Q_H and their respective PM, gain crossover frequency (ω_{gc}), and BW are listed in Table III, respectively.

From Table III, it is observed that, with the increase in Q_H, PM is increasing, but BW is decreasing. As per the specification, PM should be at least 50^o, and at the same time, the BW should be high enough so that the current loop can be made sufficiently faster than the voltage loop. Also, Q_H should be within 10 due to the limit provided by analog circuit implementation. So, Q_H= 10 is selected.

TABLE III
PM, ω_{gc} AND BW FOR DIFFERENT VALUES OF Q_H

Q_H	PM (deg.)	ω_{gc} (kHz)	BW (kHz)
5	7.39	39	58.6
10	51.30	22.5	44.7
15	62.80	17.3	32.6
20	67.30	15.10	21.6

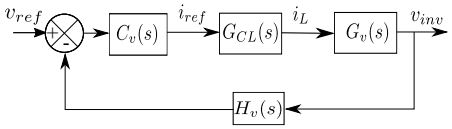


Fig. 6. Control block diagram for the outer voltage loop.

B. Design of Voltage Controller

The control block diagram of the voltage loop is shown in Fig. 6, where $C_v(s)$, $G_v(s)$ are the voltage controller and voltage loop plant, respectively. $H_v(s)$ is the voltage sensor, modeled as a simple DC gain, $H_v(s)$= α_v= 0.05. An expression for $G_v(s)$ is given in (7).

$$G_v(s) = \frac{v_{inv}(s)}{i_L(s)} = \frac{1}{C_f} \frac{s + \frac{R_{eq}}{L_l}}{s^2 + \frac{R_{eq}}{L_l}s + \frac{1}{L_f C_f}} \quad (7)$$

For a 50/60 Hz PWM inverter, the current loop bandwidth is typically designed at least a decade higher than the voltage loop. So, while designing the voltage controller, the current loop ($G_{CL}(s)$) is adequately modeled as $1\angle 0^o$. But this simplified approach is not valid for the HFAC PWM inverter since maintaining sufficient difference between the current and the voltage loop bandwidths may not be feasible. Therefore, an accurate plant model ($G_{CL}(s)G_v(s)$) is considered for voltage controller design.

Similar to the current loop, the parameters for the voltage controller are selected based on the steady-state error and stability requirements. Q_H is selected to its maximum limit, and K_i is selected accordingly without compromising stability. The control and performance parameters of both voltage and current loops are listed in Table IV. Considering these control parameters, bode plots of the plant ($G_{CL}(s)G_v(s)$) and loop gain ($C_v(s)G_{CL}(s)G_v(s)H_v$) transfer functions for the voltage loop are presented in Fig. 7.

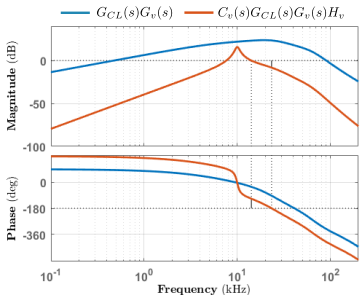


Fig. 7. Bode plot of voltage loop.

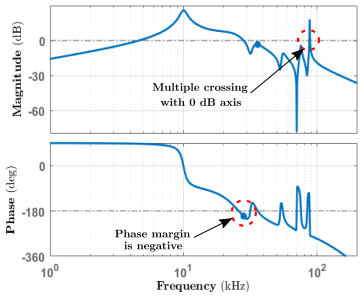


Fig. 8. Loop gain with trap filters.

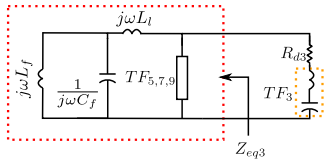


Fig. 9. Equivalent circuit of Z_{eq3} and TF_3+R_{d3}.

TABLE IV
CONTROL AND PERFORMANCE PARAMETERS.

	Control Parameters			Performance Parameters		
	K_i	Q_H	ω_o(kHz)	PM (deg.)	BW (kHz)	SS (%)
Current Controller	3	10	10^4	51.3^o	44.7	5.4
Voltage Controller	10	10	10^4	66.4^o	24.2	13.7

IV. CLOSED-LOOP CONTROLLER DESIGN WITH NON-LINEAR LOAD

The plant transfer function of the current loop considering the trap filters (Fig.2) is expressed in (8), where L_h and C_h are the h^{th} order trap filter inductor and capacitor respectively. The parameters for the trap filters are listed in Table I.

$$G_i(s) = \frac{i_L(s)}{d_{AB}(s)} = \frac{V_{DC}}{L_f} \frac{s + \frac{1}{Z_b(s)C_f}}{s^2 + \frac{s}{Z_b(s)C_f} + \frac{1}{L_f C_f}}$$
$$Z_b(s) = (sL_l) + TF_3(s)||TF_5(s)||TF_7(s)||TF_9(s)||R_{eq},$$
$$TF_h(s) = sL_h + \frac{1}{sC_h}, h = 3, 5, 7, 9. \tag{8}$$

With the control parameters listed in Table IV and the current plant in (8), the bode plot of the loop gain transfer function of the current loop is plotted in Fig. 8.

Clearly, the phase margin is negative, indicating an unstable system due to the phase loss provided by the 3^{rd} harmonic trap around 30 kHz. Also, the magnitude plot crosses the 0 dB axis multiple times with the phase angle around -180^o indicating another reason for instability. This phenomenon is caused by the notch in the gain plot at 90 kHz due to the 9^{th} harmonic trap. The possibility of introducing damper resistances in series with both 3^{rd} and 9^{th} harmonic traps is considered to address these issues. The 3^{rd} harmonic damper can potentially reduce the slope of the phase characteristic around 30 kHz. Similarly, the 9^{th} harmonic damper can lower the gain magnitude at 90 kHz. However, even after connecting the damper resistances, the 3^{rd} and 9^{th} harmonic traps should continue to offer the lowest impedance paths to the harmonic currents flowing due to the non-linear diode-bridge-rectifier load. Based on these considerations, the damper design is carried out as follows.

A. Design of Damper for 3^{rd} Harmonic Trap Filter

An equivalent circuit of the filter network for 3^{rd} harmonic trap filter is shown in Fig. 9. Here, TF_3 denotes the impedance of the 3^{rd} harmonic trap filter, R_{d3} is the combination of effective series resistance (ESR) and external damper resistance, and $TF_{5,7,9}$ is the combined impedance contributed by all other trap filters. So, $TF_3 = j\omega L_3 + (1/j\omega C_3)$ and $TF_{5,7,9} = (TF_5||TF_7||TF_9)$. The equivalent impedance, Z_{eq3} is expressed in (9).

$$Z_{eq3} = ((j\omega L_f||\frac{1}{j\omega C_f}) + j\omega L_l)||TF_{5,7,9} \tag{9}$$

Fig. 10a represents the bode plot of loop gain transfer function of current loop considering different values of damper resistances, R_{d3} in series with 3^{rd} harmonic trap. Clearly, the minimum value of R_{d3} required to get the positive phase margin is 6Ω. Fig. 10d depicts the impedance plot considering different values of R_{d3}, as shown in Fig. 9. If the value of R_{d3} is more than 1Ω, then the 3^{rd} harmonic trap filter offers higher impedance to 3^{rd} harmonic current compared to Z_{eq3}. So, deciding R_{d3} to fulfill both the design constraints is not feasible. The reduction of K_i can only improve the PM. If K_i is reduced from 3 to 1.2, the PM is noted to be improved up to 57.9^o.

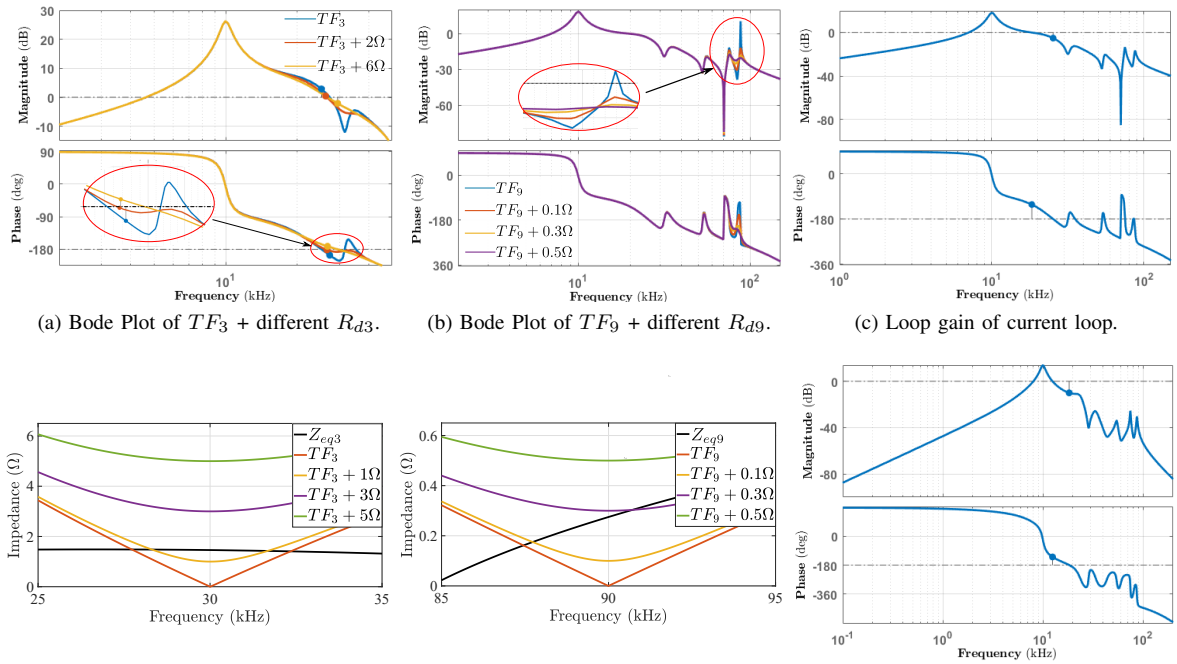
B. Design of Damper for 9^{th} Harmonic Trap Filter

Fig. 10b represents the bode plot of the current loop gain transfer function considering the different values of damper resistors, R_{d9} in series with 9^{th} harmonic trap. It is observed that, after reduction of K_i, the gain curve of the loop gain transfer function of the current loop crosses the 0 dB axis multiple times due to the notch around 90 kHz, provided by 9^{th} harmonic trap filter. The value of R_{d9}, to avoid the multiple zero-crossings in the loop gain characteristics, is $\geq$ 0.1 Ω. Similar to (8), equivalent impedance parallel to the 9th harmonic trap filter, Z_{eq9}, can be determined. Fig. 10e depicts the impedance plot of 9^{th} harmonic trap filter along with different values of R_{d9}. These impedance plots clarify that for a choice of damper around 0.1 Ω, the trap filter offers lower impedance to the 9^{th} harmonic (90 kHz) current compared to Z_{eq9} and also satisfies the stability criterion. So, both the design constraints are met.

The modified control and performance parameters of both voltage and current loop are listed in Table V. With reduced K_i and damper resistor in series with 9^{th} harmonic trap filter, the bode plot of loop gain transfer functions of current and voltage loops are shown in Fig. 10c and Fig. 10f, respectively. Clearly, both the control loops are stable.

V. ANALOG RESONANT CONTROLLER DESIGN

The op-amp-based active band-pass filter circuit (shown in Fig. 11) is used to implement the resonant controller for both



(a) Bode Plot of TF_3 + different R_{d3}. (b) Bode Plot of TF_9 + different R_{d9}. (c) Loop gain of current loop.

(d) Plot of Z_{eq3} and TF_3 + different R_{d3} (e) Plot of Z_{eq9} and TF_3 + different R_{d9} (f) Loop gain of voltage loop.

Fig. 10. Impact of introducing damper resistor on stability.

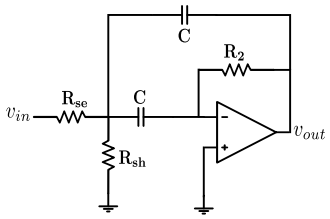
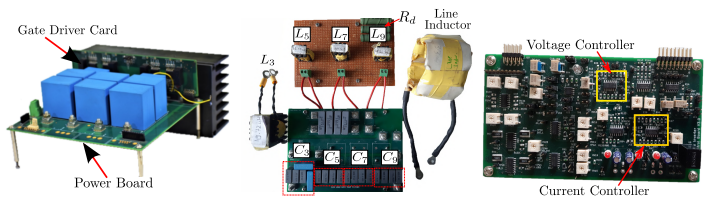


Fig. 11. Active band-pass filter.



(a) (b) (c)

Fig. 12. Experimental prototype. (a) gate driver card with power board, (b) line inductance and trap filters (c) analog control card.

TABLE V
MODIFIED CONTROL AND PERFORMANCE PARAMETERS WITH NON-LINEAR LOAD

	Control Parameters			Performance Parameters		
	K_i	Q_H	ω_o(kHz)	PM(deg.)	BW(kHz)	SS (%)
Current Controller	1.2	10	10	57.9^o	27.4	10.7
Voltage Controller	10	10	10	51.2^o	16.6	15.8

TABLE VI
CIRCUIT PARAMETERS OF RESONANT CONTROLLER

	R_2 (kΩ)	R_{se} (kΩ)	R_{sh} (kΩ)	C (nF)
Current Controller	340	135	0.784	1
Voltage Controller	318	15	0.816	1

voltage and current loops, and its transfer function is given in (10). According to the op-amp (OPA4134) datasheet, the differential capacitance is 5 pF, and C is selected 200 times higher than that to avoid any effect of OpAmp non-idealities. For an assumed value of C=1 nF, and known values of K_i, Q_H and ω_o, R_2, R_{se} and R_{sh} are selected from (11), and these parameters for voltage and current controllers are listed in TableVI.

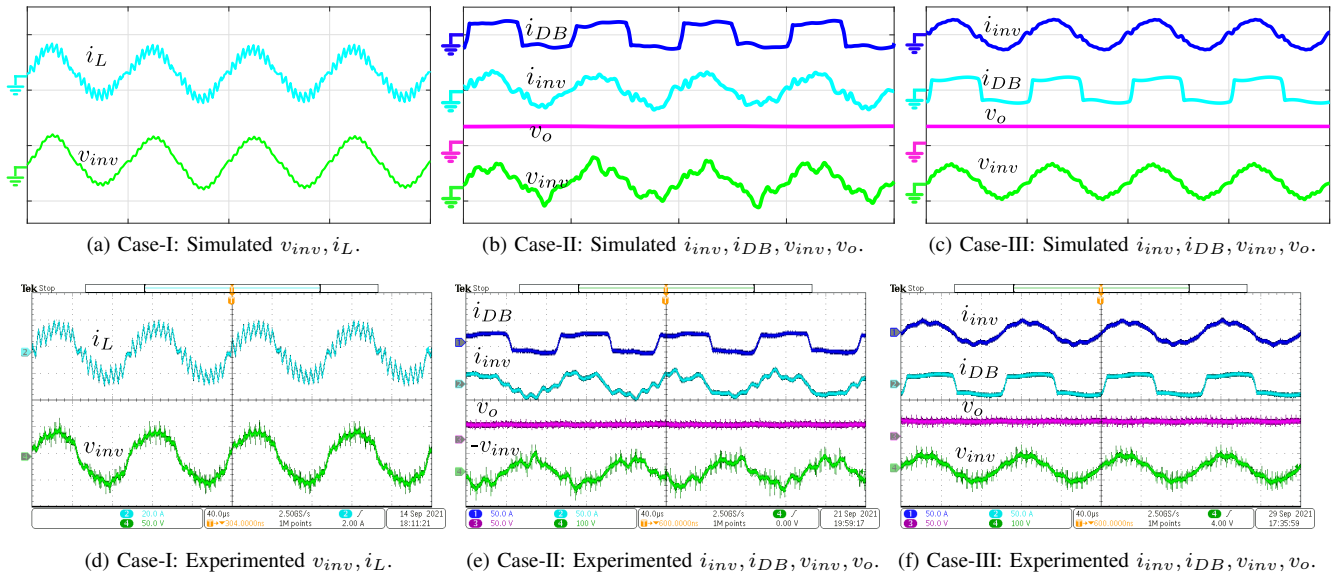
$$T_o(s) = -\frac{K_i \frac{s}{\omega_o Q_H}}{(\frac{s}{\omega_o})^2 + \frac{s}{\omega_o Q_H} + 1} \tag{10}$$

$$K_i = \frac{1}{2}\frac{R_2}{R_{se}},\ Q_H = \frac{1}{2}\sqrt{\frac{R_2}{R_{se}||R_{sh}}},\ w_o = \frac{1}{\sqrt{(R_{se}||R_{sh})R_2 C}} \tag{11}$$

VI. RESULTS AND DISCUSSION

Snapshots of the experimental prototype are shown in Fig. 12. Based on the specifications listed in Table II, a detailed loss calculation (both conduction and switching losses) is done, and the ratings of the Si-based MOSFETs (IPP075N15N3 G) are decided considering the appropriate margin. The gate driver (ADuM4135) is selected depending upon the voltage level and peak current capability. Due to the constraints of satellite power applications, in the inverter power board, all the power MOSFETs are arranged in the same row. The gate driver card is placed at the right angle to the power board and in front of the devices, as shown in Fig. 12a. The trap filters and the line inductor and analog control card are shown in Fig. 12b and Fig. 12c, respectively.

With the control parameters listed in Table IV, the closed loop is implemented with resistive load (Case-I), and its simulation and experimental results are given in Fig. 13a and Fig. 13d, respectively. The system is stable, which validates the bode plot of current and voltage loop transfer functions shown in Fig. 5b and Fig. 7, respectively. The measured value of



(a) Case-I: Simulated v_{inv}, i_L. (b) Case-II: Simulated $i_{inv}, i_{DB}, v_{inv}, v_o$. (c) Case-III: Simulated $i_{inv}, i_{DB}, v_{inv}, v_o$.

(d) Case-I: Experimented v_{inv}, i_L. (e) Case-II: Experimented $i_{inv}, i_{DB}, v_{inv}, v_o$. (f) Case-III: Experimented $i_{inv}, i_{DB}, v_{inv}, v_o$.

Fig. 13. Closed-loop operation of HFAC PWM inverter. (a) Scale: i_L (20 A/div) and v_{inv} (50 V/div); (b), (c) Scale: i_{inv} and i_{DB} (50 A/div), v_o (50 V/div) and v_{inv} (100 V/div). (d) Scale: i_L (20 A/div) and v_{inv} (50 V/div); (e), (f) Scale: i_{inv} and i_{DB} (50 A/div), v_o (50 V/div) and v_{inv} (100 V/div). X-axis: 40μs/div for simulation and experiment.

steady-state error in the experiment for voltage loop is around 7.67%.

Next, with the same control parameters (Table IV), the closed loop is run for the non-linear load (Case-II), and its simulation and experimental results are given in Fig. 13b and Fig. 13e, respectively. In this case, the v_{inv} and i_{inv} are not close to the sinusoidal waveform, and also, they are not symmetric in every power line cycle. This indicates the system is unstable and thus validates the bode plot of the current loop transfer function shown in Fig. 8.

Then, the closed loop is implemented with the modified control parameters listed in Table V for non-linear load, and its simulation and experimental results are given in Fig. 13c and Fig. 13f, respectively. Again, the system is stable. However, steady-state error for the voltage loop is compromised due to the modified control parameters, and its value is measured to be 9.54%, which finally validates the bode plots shown in Fig. 10c and Fig. 10f.

VII. Conclusion

Controller design for 1ϕ HFAC PWM inverter for satellite power applications is discussed. A systematic approach to decide the control parameters for the current and voltage loop is detailed, considering HF PWM inverter with resistive load. The steady-state error of the voltage loop is measured at around 7.67%. The current loop becomes unstable with the same control parameters when the HF inverter is operated with the non-linear load. The possibility of connecting damper resistances in series with trap filters is discussed to make the loop stable, and modification in control parameters is performed. The modified control parameters and damper resistor make the current and voltage loop stable. In this case, the steady-state error is measured at around 9.54%. The B.W of the current and voltage loop is maintained at 27.4 kHz and 16.6 kHz, respectively, which ultimately ensures the fastness of the current loop than the voltage loop. A laboratory-scale prototype is designed and fabricated to validate the proposed controller design approach at 500 W, 50 V_{peak}, 10 kHz fundamental frequency, and 200 kHz switching frequency.

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